IN THE CLAIMS:

Please cancel claims 2-4 and 6 without prejudice or disclaimer, and amend claim 5 as follows:

1-4. (Cancelled)

5. (Currently Amended) An image display device ~~according to claim 3~~ provided with an active-matrix substrate comprising:

an insulating substrate; and

a plurality of circuit regions fabricated on said insulating substrate and including at least a pixel section and a pixel-driving circuit section, each of said pixel section and said pixel-driving circuit section having a polycrystalline silicon semiconductor film,

wherein at least one of said plurality of circuit regions has a first type of a thin film transistor and a second type of a thin film transistor, and

an angular orientation of a direction of a current flowing through a channel of said first type of a thin film transistor is formed to be non-parallel with an angular orientation of a direction of a current flowing through a channel of said second type of a thin film transistor,

wherein said plurality of circuit regions includes at least one pair of a first-type circuit region constituting a first circuit and a second-type circuit region constituting a second circuit,

all thin film transistors in said first-type circuit region flow currents through channels thereof in one angular orientation, and

angular orientations of currents flowing through channels of thin film transistors in said second-type circuit region are plural in number, and

wherein, in said first-type circuit region, a peak-to-valley height difference of a surface of said channel, a source region and a drain region of said thin film transistors is equal to or smaller than 5 nm, and crystalline grains of said polycrystalline silicon semiconductor film are of a rectangular shape of 0.3 μm to 2 μm in width and 4 μm or more in length; and

in said second-type circuit region, an average crystalline grain diameter is 1 μm or smaller and a peak-to-valley height difference of a surface is equal to or greater

than 20 nm, in said channel, a source region and a drain region of said thin film transistors.

6-8. (Cancelled)

9. (Previously Presented) An image display device according to claim 5,

wherein in said polycrystalline silicon films in a channel, a source region and a drain region of said thin film transistors constituting said pixel section,

an average crystalline grain diameter is 1 μm or smaller, and

a peak-to-valley height difference of a surface is equal to or greater than 20 nm,

wherein in at least one of said plurality of circuit regions excluding said pixel section,

crystalline grains of said polycrystalline silicon films are of a rectangular shape of 0.3 μm to 2 μm in width and 4 μm or more in length in a channel, a source region and a drain region of said thin film transistors, and

a peak-to-valley height difference of a surface of said channel, said source region and said drain region of said thin film transistors is equal to or smaller than 5 nm.

10. (Previously Presented) An image display device according to claim 5, wherein said thin film transistors have plural kinds of gate insulating materials and plural kinds of thickness in ones of said plurality of circuit regions excluding said one of said plurality of circuit regions constituting said pixel section.

11. (Cancelled)

12. (Previously Presented) An image display device according to claim 5, wherein a level shifter, a sampling switch circuit and a buffer circuit constituting a pixel-driving circuit are fabricated in ones of said plurality of circuit regions excluding said one of said plurality of circuit regions constituting said pixel section,

said channel, said source region and said drain region of said thin film transistors constituting said pixel-driving circuit are formed of polycrystalline silicon

films having an average crystalline grain diameter of 1 μm or smaller and a peak-to-valley height difference of a surface equal to or greater than 20 nm, and

said channel, said source region and said drain region of said thin film transistors constituting at least one of said circuits excluding said level shifter and said sampling switch circuit are formed of polycrystalline silicon films having crystalline grains of a rectangular shape of 0.3 μm to 2 μm in width and 4 μm or more in length and a peak-to-valley height difference of a surface equal to or smaller than 5 nm.